NETWORK PARAMETER
TRANSDUCER - ANALYZER
P10 TYPE

SERIAL INTERFACE
Service manual

CONTENTS:

1. PREFACE

The programmable P10 transducer - analyzer destined to measure parameters of power networks has been provided with a serial interface in RS-485 standard to communicate with other devices.

The asynchronous communication protocol MODBUS has been implemented on this serial interface.

The configuration of serial interface parameters has been described in the Service Manual of the P10 transducer - analyzer.

Composition of serial interface parameters concerning P10 transducer:

· Transducer address	1...247
· Transmission speed	300/600/1200/2400/4800/9600/19200 bits/sec
· Working modes	ASCII, RTU
· Information unit	ASCII: 8N1, 7E1, 701
	RTU: 8N2, 8E1, 801
· Maximal response time:	600 ms

Explanation of some abbreviations:

ASCII =	American Standard Code for Information Interchange
RTU =	Remote Terminal Unit
LRC =	Longitudinal Redundancy Check
CRC =	Cyclic Redundancy Check
CR =	Carriage Return
LF =	Line -Feed (Character)
MSB =	Most - Significant Bit

2. DESCRIPTION OF THE MODBUS PROTOCOL

The MODBUS interface is a standard adopted by manufacturers of industrial controllers for an asynchronous character exchange of information between different devices of measuring and controlling systems.

It has the following features:

· Simple access rule to the interface grounded on the „master slave” principle,

· Protection of transmitted messages against errors,

· Confirmation of remote order realisation and error signalling,

· Effective actions protecting against the system suspension,

· Taking advantage of the asynchronous character transmission.

Device controllers working in the MODBUS protocol can communicate with each other and with other devices using the master - slave technique, in which only one device (the master) can initiate transactions (called „queries”).

The other devices (the slaves) respond by supplying the requested data to the master, or by taking the action requested in the query.

Typical master devices include host processors and programming pannels. Typical slaves include programmable controllers.

The master can address individual slaves, or can initiate a broadcast message to all slaves. Slaves return a message called a „response" to queries that are addressed to them individually. (Responses are not returned to broadcast queries from the master).

The MODBUS protocol establishes the format for the master's query by placing into it the device address,

a function code defining the requested action, any data to be sent, and an error checking code.

The slave's response message is also constructed using MODBUS protocol.

It contains fields confirming the action taken, any data to be returned, and an error checking code.

If an error occured in receipt of the message, or if the slave is unable to perform the requested action, the slave will construct an error message and send it as its response.

At the message level, the MODBUS protocol still applies the master - slave principle even though the network communication method is peer-to-peer.

If a controller orginates a message it does so as a master device, and expects a response from a slave device. Similarly, when a controller receives a message it constructs a slave response and returns it to the originating controller.

The format of transmitted information is as follows:

- **Master ⇒ slave:** device address, function code, data to be sent, error checking code
- **Slave ⇒ master:** sender address, confirmation, data to be sent, error checking code

Devices working in the MODBUS protocol can be setup to communicate on standard MODBUS networks using either of two transmission modes: ASCII or RTU. Users select the desired mode, along with the serial port communication parameters (baud rate, parity mode, etc) during configuration of each controller.

The mode and serial parameters must be the same for all devices on a MODBUS network.

In the MODBUS system, transmitted messages are placed into frames that are not related to serial transmission. These frames have a defined beginning and end. This enables for the receiving device to reject incomplete frames and signalling of related errors with them.

Taking into consideration the possibility to operate in one of two different transmission modes (ASCII or RTU), two frames have been defined.

2.1. ASCII framing

In the ASCII mode each byte of information is transmitted as two ASCII characters. The basic feature of this mode is that it allows to long intervals between characters within the message (to 1 sec) without causing errors.

A typical message frame is shown below.

Start	Address	Function	Data	LRC check	End index
1 char / : /	2 chars	2 chars	N chars	2 chars	2 chars CR LF

In ASCII mode messages start with a colon (:) character („:"-ASCII 3Ahex) and end with a „carriage return-line feed" (CR and LF characters).
The frame information part is protected by the code LRC (Longitudinal Redundancy Check).

2.2. RTU Framing

In RTU mode, messages start and end with a silent interval of at least 3.5 character times.
This is most easily implemented as a multiple of character times at the baud rate that is being used on the network.
The frame format is shown below:

Start	Address	Function	Data	CRC check	End index
T1-T2-T3-T4	8 bits	8 bits	N x 8bits	16 bits	T1-T2-T3-T4

Start and end indexes are marked symbolically as an interval equal to four lengths of the index (information unit). The checking code consists of 16 bits and emerges as the result of CRC calculation (Cyclical Redundancy Check) of the frame contents.

2.3. Characteristic of frame fields.

Address field

The address field of a message frame containts two characters (in ASCII mode) or eight bits (in RTU mode).
Valid slave device address are in the range of 0-247 decimal. The individual slave devices are assigned addresses in the range of 0-247. The master addresses the slave unit by placing the slave address in the frame address field. When the slave sends its response, it places its own address in this address field of the response to let the master know which slave is responding. The address 0 is used as a broadcast address recognized by all slave units connected to the bus.

Function field

The function code field of a message frame containts two characters (in ASCII mode) or eight bits (in RTU mode). Valid codes are in the range of 1-255 decimal.

When a message is sent from a master to a slave device, the function code field tells the slave what kind of action to perform. When the slave responds to the master, it uses the function code field to indicate either a normal (error-free) response or that some kind of error occured (called an exception response).

For a formal response the slave simply echoes the original function code.

For a formal response the slave returns a code that is equivalent to the original function code with its most significant logic 1.

The error code is placed on the data field of the response frame.

Data field

The data field is constructed using sets of two hexadecimal digits, in the range of 00 to FF hexadecimal.

These can be made from a pair of ASCII characters or from one RTU character, according to the network's serial transmission mode.

The data field of messages sent from a master to slave devices containts additional information which the slave must use to take the action defined by the function code. This can include items like discrete and register addresses, the quantity of items to be handled, and count of actual data bytes in the field.

The data field can be nonexistent (of zero length) in certain kinds of messages. For example, in a request from a master device for a slave to respond with its communications event log (function code 0B hexdecimal) the slave does not require any additional information. The function code alone specifies the action.

Error checking field

Two kinds of error-checking methods are used for standard MODBUS networks. The error checking field contents depends upon the method that is being used.

ASCII

When ASCII mode is used for character framing, the error checking field contains two ASCII characters. The error check characters are the result of a Longitudinal Redundancy Check (LRC) calculation that is performed on the message contents, exclusive of the beginning „colon” and terminating CRLF characters. LRC characters are appended to the message as the last field preceding the CRLF characters.

RTU

When RTU mode is used for character framing, the error checking field containts a 16-bit value implemented as two 8-bit bytes. The error check value is the result of a Cyclical Redundancy Check calculation performed on a message contents.

The CRC field is appended to the message as the last field in the message. When this is done, the low-order byte of the field is appended first, followed by the high-order byte.

The CRC high-order byte is the last byte to be sent in the message.

2.4. LRC checking

The LRC is calculated by adding together sucessIve 8-bit bytes of the message, discarding any carries, and then two is complementing the result. It is performed on the ASCII message field contents excluding the „colon" character that begins the message, and excluding the CR, LF pair at the end of the message.

The 8-bit value of the LRC sum is placed at the frame end as two ASCII characters, first the character containing the higher tetrad, and after it, the character containing the lower LRC tetrad.

2.5. CRC checking

The generating procedure of CRC is realized according the following algorythm:

1. Load a 16-bit register with FFFF hex. Call this the CRC register.
2. Exclusive OR the first 8-bit byte of the message with the low-order byte of the 16 bit CRC register, putting the result in the CRC register.
3. Shift the CRC register one bit to the right (towards the LSB), zero-filling the MSB. Extract and examine the LSB.
4. (If the LSB was 0): Repeat step 3 (another shift)

   (If the LSB was 1): Exclusive OR the CRC register with the polynomial value A001 hex.
5. Repeat steps 3 and 4 until 8 shifts have been performed.

   When this is done, a complete 8-bit byte will have been processed.
6. Repeat steps 2 through 5 for the next 8-bit byte of the message.

   Continue doing this until all bytes have been processed.
7. The final contents of the CRC register is the CRC value.
8. When the CRC is placed into the message, its upper and lower bytes must be swapped as described below.

2.6. Character formation during serial transmission

In the MODBUS protocol, characters are transmitted from the lowest to the highest bit.

Organization of the information unit in the ASCII mode:

· 1 start bit,

· 7 data field bits,

· 1 even parity check bit (odd) or lack of even parity check bit,

· 1 stop bit at even parity check or 2 stop bits when lack of even parity check.

Organization of the information unit in the RTU mode:
- 1 start bit,
- 8 data field bits,
- 1 even parity check bit (odd) or lack of even parity check bit,
- 1 stop bit at even parity check or 2 stop bits when lack of even parity check.

2.7. Transaction interruption

In the master unit the user sets up the important parameter which is the „maximal response time on the query frame" after which exceeding, the transaction is interrupted.

This time is choice such that each slave unit working in the system (even the slowest,) normally will have the time to answer to the frame query.

An exceeding of this time attests therefore about an error and such is treated by the master unit.

If the unit slave will find out a transmission error it does not accomplish the order and does not send any answer. That causes an exceeding of the waiting time after the query frame and the transaction interruption.

In the P10 transducer „the maximal response time on the query frame" is 600ms.

3. FUNCTION DESCRIPTION

In the P10 transducer-analyser following protocol functions has been implemented:

Code	Signification
03	Reading of n-register
06	Writing of an individual register
16	Writing of n-registers
17	Slave device identification

3.1. Reading of n-registers (code 03)

Demand:

The function enables the reading of values included in registers in being addressed slave device. Registers are 16 or 32-bit units, which can include numerical values bounded with changeable processes, and the like.

The demand frame defines the 16-bit start address and the number of registers to read-out.

The signification of the register contents with address data can be different for different device types.

The function is not accessible in the broadcast mode.

Example: Reading of 3 registers beginning by the register with the 6Bhex address.

Address	Function	Register address Hi	Register address Lo	Number of registers Hi	Number of registers Lo	Checking sum
01	03	00	6B	00	03	

Answer:

Register data are packing beginning from the smallest address: first the higher byte, then the lower register byte.

Example: the answer frame

Address	Function	Number of bites	Value in the regist. 107 Hi	Value in the register 108 Lo	Value in the register 108 Hi	Value in the register 109 Lo	Value in the register 109 Hi	Value sum Lo	Checking
01	03	06	02	2B	00	00	00	64	

3.2. Writing of values in the register (code 06)

Demand:

The function enables the modification of the register contents.

It is accessible in the broadcast mode.

Example

Address	Function	Register address Hi	Register address Lo	Value Hi	Value Lo	Checking sum
11	06	00	87	03	9 E	

Answer:

The correct answer to a record requirement in the register is the retransmission of the message after accomplishing the operation.

Address	Function	Register address Hi	Register address Lo	Value Hi	Value Lo	Checking sum
11	06	00	87	03	9 E	

3.3. Writing in n-registers (code 16)

Demand:

The function is accessible in broadcast mode. It enables the modification of the register contents.

Example: Writing of two registers beginning from the register adressed 136.

Address	Function	Register address Hi	Register address Lo	Number of registers Hi	Number of registers Lo	Number of bytes	Data Hi	Data Lo	Data Hi	Data Lo	Checking sum olna
01	10	00	87	00	02	04	00	0A	01	02	

Answer:

The correct answer includes the unit slave address, function code, starting address and the number of recorded registers.

Example

Address	**Function**	**Register address Hi**	**Register address Lo**	**Number of registers Hi**	**Number of registers Lo**	**Checking sum**
01	10	00	87	00	02	

3.4. Report identifying the device (code 17)

Demand:

This function enables the user to obtain information about the device type, status and configuration depending on this.

Example

Address	**Function**	**Checking Sum**
01	11	

Answer:

The field „Device identificator" in the answer frame means the unique identificator of this class of device, however the other fields include parameters depended on the device type.

Example concerning the P10 transducer

Slave address	**Function**	**Number of bytes**	**Device identificator**	**Device state**	**Voltage range**	**Current sum**	**Checking sum**
01	11	6	55	FF	0064	0001	

4. ERROR CODES

When the master device is broadcasting a demand to the slave device then, except for messages in the broadcast mode, it expects a correct answer. After sending the demand of the master unit, one of the four possibilities can occur:

· If the slave unit receives the demand without a transmission error and can execute it correctly, then it returns a correct answer,

· If the slave unit does not receive the demand, no answer is returned. Timeout conditions for the demand will be fulfilled in the master device programme.

· If the slave unit receives the demand, but with transmission errors (even parity error of checking sum LRC or CRC), no answer is returned. Timeout conditions for the demand will be fulfilled in the master device programme.

· If the slave unit receives the demand without a transmission error but does not execute it correctly (e.g. if the demand is, the reading-out of a non-existent bit output or register), then it returns the answer including the error code, informing the master device about the error reason.

· A message with an incorrect answer includes two fields distinguishing it from the correct answer.

The function code field:

In the correct answer, the slave unit retransmits the function code from the demand message in the field of the answer function code. All function codes have the most-significant bit (MSB) equal zero (code values are under 80h). In the incorrect answer, the slave unit sets up the MSB bit of the function code at 1.

This causes that the function code value in the incorrect answer is exactly 80h greater than it would be in a correct answer.

On the base of the function code with a set up MSB bit the programme of the master device can recognize an incorrect answer and can check the error code on the data field.

The data field:

In a correct answer the slave device can return data to the data field (certain information required by the master unit). In the incorrect answer the slave unit returns the error code to the data field. It defines conditions of the slave device which had produced the error.

An example considering a demand of a master device and the incorrect answer of the slave unit has been shown below. Data are in the hexadecimal shape.

Example: demand

Slave address	**Function**	**Variable address Hi**	**Variable address Lo**	**Number of variables Hi**	**Number of variables Lo**	**Checking sum**
0A	01	04	A1	00	01	

Example: incorrect answer

Slave	Function	Error	Checking
0A	81	02	

In this example the master device addresses the demand to the slave unit with No10 (0Ah). The function code (01) serves to the read-out operation of the bit input state. Then this frame means the demand of the status read-out of a one bit input with the address number: 1245 (04A1h).

If in the slave device there is no bit input with the given address, then the device returns the incorrect answer with the No 02 error code. This means a forbidden data address in the slave device. Possible error codes and their meanings are shown in the table below.

Code	Meaning
01	Forbidden function
02	Forbidden data address
03	Forbidden data value
04	Damage in the connected device
05	Confirmation
06	Occupied, message removed
07	Negative confirmation
08	Error of memory parity

5. REGISTER MAP OF THE P10 TRANSDUCER - ANALYZER

Data included in the P10 transducer - analyzer are located in 16-bit or 32-bit registers. Process variables and meter parameters are placed in the register addresses area in a way depending on the variable value type. Bits in the 16-bit register are numbered from the lowest to the highest ones (b0-b15).

32-bit registers include float numbers in the IEEE-745 standard.

The register map has been devided into the following areas.

Address range	Value type	Description
4000 - 4039	Integer (16 bits)	The value is placed in one 16-bit register. **Table 1** includes the register description. Registers can be read out and recorded.
7500 - 7924	Float (32 bits)	The value is placed in the 32-bit register. The description of registers is included in **Table 2**. Registers are only to be read-out.

Contents of 16-bit registers with addresses from 4000 to 4039.

Table 1

Item	Address	Symbol	Range	Description
1	4000	I Ratio	1...20000	Current transformer ratio
2	4001	U Ratio	1...4000	Voltage transformer ratio
3	4002	Clear E*t?	0, 1	Tariff counter clearing
4	4003	Clear Pav?	0, 1	Pav power clearing (e.g. 15 min.) Pav (Max and Min values)
5	4004	Pav Time?	1, 2, 3	Averaging time of Pav power
6	4005	Pav Window	0, 1	Synchronization of Pav power averaging by means of: - clock - moving window
7	4006	Password	0000...9999	Access code change
8	4007	Alarm 1 Parameter	Code acc. table 8 Service manual	Two-state output 2-quantity
9	4008	Alarm 1 On	-120...0...120 (%)	Two-state output 1 Switch-on value
10	4009	Alarm 1 Off	-120...0...120 (%)	Two-state output 1 Switch-off value
11	4010	Alarm 2 Parameter	Code acc. table 8 Service manual	Two-state output 2 - quantity
12	4011	Alarm 2 On	-120...0...120 (%)	Two-state output 2 Switch-on value
13	4012	Alarm 2 Off	-120...0...120 (%)	Two-state output 2
14	4013	Alarm 3 Parameter	Code acc. table 8 Service manual	Two-state output 3 - quantity
15	4014	Alarm 3 On	-120...0...120 (%)	Two-state output 3 Switch-on value
16	4015	Alarm 3 Off	-120...0...120 (%)	Two-state output 3 Switch-off value
17	4016	Alarm 4 Parameter	Code acc. table 8 Service manual	Two-state output 4 - quantity
18	4017	Alarm 4 On	-120...0...120 (%)	Two-state output 4 Switch-on value

Table 1 (continuation)

Item	Address	Symbol	Range	Description
19	4018	Alarm 4 Off	-120...0...120 (%)	Two-state output 4 Switch-off value
20	4019	Alarms Delay	0...100	Delay of alarm activity
21	4020	AnOut1 Parameter	Code acc. table 8 Service manual	Quantity on continuous output No 1
22	4021	AnOut1 Low (%)	-120...0...120 (%)	Lower value of input range No 1
23 24	4022 4023	AnOut1 Hi (%) AnOut1 Zero (mA)	-120...0...120 0, 1, 5, 10	Upper value of input range No 1 Type of analog output No 1
25	4024	AnOut2 Parameter	Code acc. table 8 Service manual	Quantity on continuous output No 2
26	4025	AnOut2 Low (%)	-120...0...120 (%)	Lower value of input range No 2
27	4026	AnOut2 Hi (%)	-120...0...120	Upper value of input range No 2
28	4027	AnOut2 Zero (mA)	0, 1, 5, 10	Type of analog output No 2
29	4028	AnOut3 Parameter	Code acc. table 8 Service manual	Quantity on continuous output No 3
30	4029	AnOut3 Low (%)	-120...0...120 (%)	Lower value of input range No 3
31	4030	AnOut2 Hi (%)	-120...0...120	Upper value of input range No 3
32	4031	AnOut2 Zero (mA)	0, 1, 5, 10	Type of analog output No 3
33	4032	AnOut4 Parameter	Code acc. table 8 Service manual	Quantity on continuous output No 4
34	4033	AnOut4 Low (%)	-120...0...120 (%)	Lower value of input range No 4
35	4034	AnOut4 Hi (%)	-120...0...120	Upper value of input range No 4
36	4035	AnOut4 Zero (mA)	0, 1, 5, 10	Type of analog output No 4
37	4036	Year		Year
38	4037	MonthDay		Month* 100 + day
39	4038	HourMin		Hour* 100 + minute
40	4039	Alarm	0...16	State of relay outputs b0, b1, b2, b3

Contents of 32-bit registers with addresses from 7500 to 7619

Table 2

Item	Register	Symbol	Unit	Unit name
0				Without quantity - display extincted
1	7500	U1	V	L1 phase voltage
2	7501	I1	A	L1 phase current
3	7502	P1	W	L1 phase active power
4	7503	Q1	Var	L1 phase reactive power
5	7504	S1	VA	L1 phase apparent power
6	7505	Pf1		L1 phase active power factor
7	7506	tφ1		L1 phase reactive power over the active power
8	7507	U2	V	L2 phase voltage
9	7508	I2	A	L2 phase current
10	7509	P2	W	L2 phase active power
11	7510	Q2	Var	L2 phase reactive power
12	7511	S2	VA	L2 phase apparent power
13	7512	Pf2		L2 phase active power factor
14	7513	tφ2		L2 phase reactive power over the active power
15	7514	U3	V	L3 phase voltage
16	7515	I3	A	L3 phase current
17	7516	P3	W	L3 phase active power
18	7517	Q3	Var	L3 phase reactive power
19	7518	S3	VA	L3 phase apparent power
20	7519	Pf3		L3 phase active power factor
21	7520	tφ3		L3 phase reactive power over the active power
22	7521	Us	V	Mean three-phase voltage
23	7522	Is	A	Mean three-phase current
24	7523	P	W	Three-phase active power
25	7524	Q	Var	Three-phase reactive power
26	7525	S	VA	Three-phase apparent power
27	7526	Pf		Active power factor
28	7527	tφ		Mean - Three-phase reactive power over the three-phase active power - tφ = Q/P
29	7528	f	Hz	Frequency
30	7529	U12	V	L1-L2 phase-to-phase voltage
31	7530	U23	V	L2-L3 phase-to-phase voltage

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
32	7531	U31	V	L3-L1 phase-to-phase voltage
33	7532	U123	V	Mean phase-to-phase voltage
34	7533	PAV	W	(e.g.) 15-minute mean active power
35	7540			Date - day, month
36	7541			Date-year
37	7542			Time- hours, minutes
38	7543			Time-secondes
39	7544, 7545	U1	V	L1 phase voltage - min, max
40	7546, 7547	U2	V	L2 phase voltage - min, max
41	7548, 7549	U3	V	L3 phase voltage - min, max
42	7550, 7551	I1	A	L1 phase current - min, max
43	7552, 7553	I2	A	L2 phase current - min, max
44	7554,7555	I3	A	L3 phase current - min, max
45	7556, 7557	P1	W	L1 phase active power - min, max
46	7558, 7559	P2	W	L2 phase active power - min, max
47	7560, 7561	P3	W	L3 phase active power - min, max
48	7562, 7563	S1	VA	L1 phase apparent power - min, max
49	7564, 7565	S2	VA	L2 phase apparent power - min, max
50	7566, 7567	S3	VA	L3 phase apparent power - min, max
51	7568, 7569	Q1	VAr	L1 phase reactive power - min, max
52	7570, 7571	Q2	VAr	L2 phase reactive power - min, max
53	7572, 7573	Q3	VAr	L3 phase reactive power - min, max
54	7574, 7575	Pf1		L1 phase active power factor - min, max
55	7576, 7577	Pf2		L2 phase active power factor - min, max
56	7578, 7579	Pf3		L3 phase active power factor - min, max
57	7580, 7581	tφ1		tφ1 = Q1/P1, L1 phase - min, max
58	7582, 7583	tφ2		tφ2 = Q2/P2, L2 phase - min, max
59	7584, 7585	tφ3		tφ3 = Q3/P3, L3 phase - min, max
60	7586, 7587	US	V	Mean three-phase voltage - min, max
61	7588, 7589	IS	A	Mean three-phase current - min, max
62	7590, 7591	P	W	Three-phase active power - min, max
63	7592, 7593	Q	VAr	Three-phase reactive power - min, max

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
64	7594, 7595	S	VA	Three-phase apparent power - min, max
65	7596, 7597	Pf	Pf	Active power factor - min, max
66	7598, 7599	tφ		Mean three-phase reactive power factor over active power factor - min, max
67	7600, 7601	f	Hz	Frequency - min, max
68	7602, 7603	U12	V	L1-L2 phase-to-phase voltage - min, max
69	7604, 7605	U23	V	L2-L3 phase-to-phase voltage - min, max
70	7606, 7607	U31	V	L3-L1 phase-to-phase voltage - min, max
71	7608, 7609	U123	V	Mean phase-to-phase voltage - min, max
72	7610, 7611	PAV	W	(e.g.) 15 minute mean active power) - min, max
73	7612	THD_{U1}	%	THD of the L1 phase voltage
74	7613	THD_{U2}	%	THD of the L2 phase voltage
75	7614	THD_{U3}	%	THD of the L3 phase voltage
76	7615	THD_{U1}	%	THD of the L1 phase current
77	7616	THD_{U2}	%	THD of the L2 phase current
78	7617	THD_{U3}	%	THD of the L3 phase current
79	7618, 7619	THD_{U1}	%	THD of the L1 phase voltage - min, max
80	7620, 7621	THD_{U2}	%	THD of the L2 phase voltage - min, max
81	7622, 7623	THD_{U3}	%	THD of the L3 phase voltage - min, max
82	7624, 7625	THD_{U1}	%	THD of the L1 phase current - min, max
83	7626, 7627	THD_{U2}	%	THD of the L2 phase current - min, max
84	7628, 7629	THD_{U3}	%	THD of the L3 phase current - min, max
85	7630	HarU1 (1)	%	1-st harmonic of L1 phase voltage
86	7631	HarU1 (2)	%	2-nd harmonic of L1 phase voltage
87	7632	HarU1 (3)	%	3-rd harmonic of L1 phase voltage
88	7633	HarU1 (4)	%	4-th harmonic of L1 phase voltage
89	7634	HarU1 (5)	%	5-th harmonic of L1 phase voltage
90	7635	HarU1 (6)	%	6-th harmonic of L1 phase voltage
91	7636	HarU1 (7)	%	7-th harmonic of L1 phase voltage
92	7637	HarU1 (8)	%	8-th harmonic of L1 phase voltage
93	7638	HarU1 (9)	%	9-th harmonic of L1 phase voltage
94	7639	HarU1 (10)	%	10-th harmonic of L1 phase voltage
95	7640	HarU1 (11)	%	11-th harmonic of L1 phase voltage
96	7641	HarU1 (12)	%	12-th harmonic of L1 phase voltage

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
97	7642	HarU1 (13)	%	13-th harmonic of L1 phase voltage
98	7643	HarU1 (14)	%	14-th harmonic of L1 phase voltage
99	7644	HarU1 (15)	%	15-th harmonic of L1 phase voltage
100	7645	HarU1 (16)	%	16-th harmonic of L1 phase voltage
101	7646	HarU1 (17)	%	17-th harmonic of L1 phase voltage
102	7647	HarU1 (18)	%	18-th harmonic of L1 phase voltage
103	7648	HarU1 (19)	%	19-th harmonic of L1 phase voltage
104	7649	HarU1 (20)	%	20-th harmonic of L1 phase voltage
105	7650	HarU1 (21)	%	21-st harmonic of L1 phase voltage
106	7651	HarU1 (22)	%	22-nd harmonic of L1 phase voltage
107	7652	HarU1 (23)	%	23-rd harmonic of L1 phase voltage
108	7653	HarU1 (24)	%	24-th harmonic of L1 phase voltage
109	7654	HarU1 (25)	%	25-th harmonic of L1 phase voltage
110	7655	HarU2 (1)	%	1-st harmonic of L2 phase voltage
111	7656	HarU2 (2)	%	2-nd harmonic of L2 phase voltage
112	7657	HarU2 (3)	%	3-rd harmonic of L2 phase voltage
113	7658	HarU2 (4)	%	4-th harmonic of L2 phase voltage
114	7659	HarU2 (5)	%	5-th harmonic of L2 phase voltage
115	7660	HarU2 (6)	%	6-th harmonic of L2 phase voltage
116	7661	HarU2 (7)	%	7-th harmonic of L2 phase voltage
117	7662	HarU2 (8)	%	8-th harmonic of L2 phase voltage
118	7663	HarU2 (9)	%	9-th harmonic of L2 phase voltage
119	7664	HarU2 (10)	%	10-th harmonic of L2 phase voltage
120	7665	HarU2 (11)	%	11-th harmonic of L2 phase voltage
121	7666	HarU2 (12)	%	12-th harmonic of L2 phase voltage
122	7667	HarU2 (13)	%	13-th harmonic of L2 phase voltage
123	7668	HarU2 (14)	%	14-th harmonic of L2 phase voltage
124	7669	HarU2 (15)	%	15-th harmonic of L2 phase voltage
125	7670	HarU2 (16)	%	16-th harmonic of L2 phase voltage
126	7671	HarU2 (17)	%	17-th harmonic of L2 phase voltage
127	7672	HarU2 (18)	%	18-th harmonic of L2 phase voltage
128	7673	HarU2 (19)	%	19-th harmonic of L2 phase voltage
129	7674	HarU2 (20)	%	20-th harmonic of L2 phase voltage
130	7675	HarU2 (21)	%	21-st harmonic of L2 phase voltage
131	7676	HarU2 (22)	%	22-nd harmonic of L2 phase voltage

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
132	7677	HarU2 (23)	%	23-rd harmonic of L2 phase voltage
133	7678	HarU2 (24)	%	24-th harmonic of L2 phase voltage
134	7679	HarU2 (25)	%	25-th harmonic of L2 phase voltage
135	7680	HarU3 (1)	%	1-st harmonic of L3 phase voltage
136	7681	HarU3 (2)	%	2-nd harmonic of L3 phase voltage
137	7682	HarU3 (3)	%	3-rd harmonic of L3 phase voltage
138	7683	HarU3 (4)	%	4-th harmonic of L3 phase voltage
139	7684	HarU3 (5)	%	5-th harmonic of L3 phase voltage
140	7685	HarU3 (6)	%	6-th harmonic of L3 phase voltage
141	7686	HarU3 (7)	%	7-th harmonic of L3 phase voltage
142	7687	HarU3 (8)	%	8-th harmonic of L3 phase voltage
143	7688	HarU3 (9)	%	9-th harmonic of L3 phase voltage
144	7689	HarU3 (10)	%	10-th harmonic of L3 phase voltage
145	7690	HarU3 (11)	%	11-th harmonic of L3 phase voltage
146	7691	HarU3 (12)	%	12-th harmonic of L3 phase voltage
147	7692	HarU3 (13)	%	13-th harmonic of L3 phase voltage
148	7693	HarU3 (14)	%	14-th harmonic of L3 phase voltage
149	7694	HarU3 (15)	%	15-th harmonic of L3 phase voltage
150	7695	HarU3 (16)	%	16-th harmonic of L3 phase voltage
151	7696	HarU3 (17)	%	17-th harmonic of L3 phase voltage
152	7697	HarU3 (18)	%	18-th harmonic of L3 phase voltage
153	7698	HarU3 (19)	%	19-th harmonic of L3 phase voltage
154	7699	HarU3 (20)	%	20-th harmonic of L3 phase voltage
155	7700	HarU3 (21)	%	21-st harmonic of L3 phase voltage
156	7701	HarU3 (22)	%	22-nd harmonic of L3 phase voltage
157	7702	HarU3 (23)	%	23-rd harmonic of L3 phase voltage
158	7703	HarU3 (24)	%	24-th harmonic of L3 phase voltage
159	7704	HarU3 (25)	%	25-th harmonic of L3 phase voltage
160	7705	HarI1 (1)	%	1-st harmonic of L1 phase current
161	7706	HarI1 (2)	%	2-nd harmonic of L1 phase current
162	7707	HarI1 (3)	%	3-rd harmonic of L1 phase current
163	7708	HarI1 (4)	%	4-th harmonic of L1 phase current
164	7709	HarI1 (5)	%	5-th harmonic of L1 phase current
165	7710	HarI1 (6)	%	6-th harmonic of L1 phase current
166	7711	HarI1 (7)	%	7-th harmonic of L1 phase current
167	7712	HarI1 (8)	%	8-th harmonic of L1 phase current

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
160	7705	HarI1 (1)	%	1-st harmonic of L1 phase current
161	7706	HarI1 (2)	%	2-nd harmonic of L1 phase current
162	7707	HarI1 (3)	%	3-rd harmonic of L1 phase current
163	7708	HarI1 (4)	%	4-th harmonic of L1 phase current
164	7709	HarI1 (5)	%	5-th harmonic of L1 phase current
165	7710	HarI1 (6)	%	6-th harmonic of L1 phase current
166	7711	HarI1 (7)	%	7-th harmonic of L1 phase current
167	7712	HarI1 (8)	%	8-th harmonic of L1 phase current
168	7713	HarI1 (9)	%	9-th harmonic of L1 phase current
169	7714	HarI1 (10)	%	10-th harmonic of L1 phase current
170	7715	HarI1 (11)	%	11-th harmonic of L1 phase currrent
171	7716	HarI1 (12)	%	12-th harmonic of L1 phase current
172	7717	HarI1 (13)	%	13-th harmonic of L1 phase current
173	7718	HarI1 (14)	%	14-th harmonic of L1 phase current
174	7719	HarI1 (15)	%	15-th harmonic of L1 phase current
175	7720	HarI1 (16)	%	16-th harmonic of L1 phase current
176	7721	HarI1 (17)	%	17-th harmonic of L1 phase current
177	7722	HarI1 (18)	%	18-th harmonic of L1 phase current
178	7723	HarI1 (19)	%	19-th harmonic of L1 phase current
179	7724	HarI1 (20)	%	20-th harmonic of L1 phase current
180	7725	HarI1 (21)	%	21-st harmonic of L1 phase current
181	7726	HarI1 (22)	%	22-nd harmonic of L1 phase current
182	7727	HarI1 (23)	%	23-rd harmonic of L1 phase current
183	7728	HarI1 (24)	%	24-th harmonic of L1 phase current
184	7729	HarI1 (25)	%	25-th harmonic of L1 phase current
185	7730	HarI2 (1)	%	1-st harmonic of L2 phase current
186	7731	HarI2 (2)	%	2-nd harmonic of L2 phase current
187	7732	HarI2 (3)	%	3-rd harmonic of L2 phase current
188	7733	HarI2 (4)	%	4-th harmonic of L2 phase current
189	7734	HarI2 (5)	%	5-th harmonic of L2 phase current
190	7735	HarI2 (6)	%	6-th harmonic of L2 phase current
191	7736	HarI2 (7)	%	7-th harmonic of L2 phase current
192	7737	HarI2 (8)	%	8-th harmonic of L2 phase current
193	7738	HarI2 (9)	%	9-th harmonic of L2 phase current
194	7739	HarI2 (10)	%	10-th harmonic of L2 phase current
195	7740	HarI2 (11)	%	11-th harmonic of L2 phase current

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
196	7741	HarI2 (12)	%	12-th harmonic of L2 phase current
197	7742	HarI2 (13)	%	13-th harmonic of L2 phase current
198	7743	HarI2 (14)	%	14-th harmonic of L2 phase current
199	7744	HarI2 (15)	%	15-th harmonic of L2 phase current
200	7745	HarI2 (16)	%	16-th harmonic of L2 phase current
201	7746	HarI2 (17)	%	17-th harmonic of L2 phase current
202	7747	HarI2 (18)	%	18-th harmonic of L2 phase current
203	7748	HarI2 (19)	%	19-th harmonic of L2 phase current
204	7749	HarI2 (20)	%	20-th harmonic of L2 phase current
205	7750	HarI2 (21)	%	21-st harmonic of L2 phase current
206	7751	HarI2 (22)	%	22-nd harmonic of L2 phase current
207	7752	HarI2 (23)	%	23-rd harmonic of L2 phase current
208	7753	HarI2 (24)	%	24-th harmonic of L2 phase current
209	7754	HarI2 (25)	%	25-th harmonic of L2 phase current
210	7755	HarI3 (1)	%	1-st harmonic of L3 phase current
211	7756	HarI3 (2)	%	2-nd harmonic of L3 phase current
212	7757	HarI3 (3)	%	3-rd harmonic of L3 phase current
213	7758	HarI3 (4)	%	4-th harmonic of L3 phase current
214	7759	HarI3 (5)	%	5-th harmonic of L3 phase current
215	7760	HarI3 (6)	%	6-th harmonic of L3 phase current
216	7761	HarI3 (7)	%	7-th harmonic of L3 phase current
217	7762	HarI3 (8)	%	8-th harmonic of L3 phase current
218	7763	HarI3 (9)	%	9-th harmonic of L3 phase current
219	7764	HarI3 (10)	%	10-th harmonic of L3 phase current
220	7765	HarI3 (11)	%	11-th harmonic of L3 phase current
221	7766	HarI3 (12)	%	12-th harmonic of L3 phase current
222	7767	HarI3 (13)	%	13-th harmonic of L3 phase current
223	7768	HarI3 (14)	%	14-th harmonic of L3 phase current
224	7769	HarI3 (15)	%	15-th harmonic of L3 phase current
225	7770	HarI3 (16)	%	16-th harmonic of L3 phase current
226	7771	HarI3 (17)	%	17-th harmonic of L3 phase current
227	7772	HarI3 (18)	%	18-th harmonic of L3 phase current
228	7773	HarI3 (19)	%	19-th harmonic of L3 phase current
229	7774	HarI3 (20)	%	20-th harmonic of L3 phase current
230	7775	HarI3 (21)	%	21-st harmonic of L3 phase current

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
231	7776	HarI3 (22)	%	22-nd harmonic of L3 phase current
232	7777	HarI3 (23)	%	23-rd harmonic of L3 phase current
233	7778	HarI3 (24)	%	24-th harmonic of L3 phase current
234	7779	HarI3 (25)	%	25-th harmonic of L3 phase current
235	7780	Ept1		1-st rate of active energy counter
236	7781	Ept2		2-nd rate of active energy counter
237	7782	Ept3		3-rd rate of active energy counter
238	7783	Ept4		4-th rate of active energy counter
239	7784	Eqt1		1-st rate of reactive energy counter
240	7785	Eqt2		2-nd rate of reactive energy counter
241	7786	Eqt3		3-rd rate of reactive energy counter
242	7787	Eqt4		4-th rate of reactive energy counter
243	7788	Est1		1-st rate of apparent energy counter
244	7789	Est1		2-nd rate of apparent energy counter
245	7790	Est1		3-rd rate of apparent energy counter
246	7791	Est1		4-th rate of apparent energy counter
253	7844, 7845	U1		Occurence time of min and max for L1 phase voltage
254	7846, 7847	U2		Occurence time of min and max for L2 phase voltage
255	7848, 7849	U3		Occurence time of min and max for L3 phase voltage
256	7850, 7851	I1		Occurence time of min and max for L1 phase current
257	7852, 7853	I2		Occurence time of min and max for L2 phase current
258	7854, 7855	I3		Occurence time of min and max for L3 phase current
259	7856, 7857	P1		Occurence time of min and max for L1 phase active power
260	7858, 7859	P2		Occurence time of min and max for L2 phase active power
261	7860, 7861	P3		Occurence time of min and max for L3 phase active power
262	7862, 7863	Q1		Occurence time of min and max for L1 phase reactive power
263	7864, 7865	Q2		Occurence time of min and max for L2 phase reactive power
264	7866, 7867	Q3		Occurence time of min and max for L3 phase reactive power

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
265	7868, 7869	S1		Occurence time of min and max for L1 phase apparent power
266	7870, 7871	S2		Occurence time of min and max for L2 phase apparent power
267	7872, 7873	S3		Occurence time of min and max for L3 phase apparent power
268	7874, 7875	Pf1		Occurence time of min and max for L1 phase active power factor
269	7876, 7877	Pf2		Occurence time of min and max of L2 phase active power factor
270	7878, 7879	Pf3		Occurence time of min and max of L3 phase active power factor
271	7880, 7881	tgφ1		Occurence time of min and max of the reactive power over the active power for the L1 phase
272	7882, 7883	tgφ2		Occurence time of min and max of the reactive power over the active power for the L2 phase
273	7884, 7885	tgφ3		Occurence time of min and max of the reactive power over the active power for the L3 phase
274	7886, 7887	U		Occurence time of min and max average three-phase voltage
275	7888, 7889	I		Occurence time of min and max average three-phase current
276	7890, 7891	P		Occurence time of min and max 3-phase active power
277	7892, 7893	Q		Occurence time of min and max 3-phase reactive power
278	7894, 7895	S		Occurence time of min and max 3-phase apparent power
279	7896, 7897	Pf		Occurence time of min and max power factor
280	7898, 7899	tgφ		Occurence time of min and max reactive power over 3-phase average active power
281	7900, 7901	f		Occurence time of min and max frequency
282	7902, 7903	U12		Occurence time of min and max phase-to-phase voltage L1 - L2

Table 2 (continuation)

Item	Register address	Symbol	Unit	Unit name
283	7904, 7905	U23		Occurence time of min and max phase-to-phase voltage L2 - L3
284	7906, 7907	U31		Occurence time of min and max phase-to-phase voltage L3 - L1
285	7908, 7909	U123		Occurence time of min and max phase-to-phase average voltage
286	7910, 7911	Pav		Occurence time of min and max 15-minut active power
287	7912, 7913	HU1		Occurence time of min and max THD for L1 phase voltage
288	7914, 7915	HU2		Occurence time of min and max THD for L2 phase voltage
289	7916, 7917	HU3		Occurence time of min and max THD for L3 phase voltage
290	7918, 7919	HI1		Occurence time of min and max THD for L1 phase current
291	7920, 7921	HI2		Occurence time of min and max THD for L2 phase current
292	7922, 7923	HI3		Occurence time of min and max THD for L3 phase current

APPENDIX A
CALCULATION OF THE CHECKSUM

In this appendix some examples of function in the C language calculating the LRC checking sum for ASCII mode and the CRC checking sum for the RTU mode have been shown.

The function for LRC calculation has two arguments:

unsigned char outMSg;*	· Pointer for the communication buffer, including binary data from which one must calculate LRC.
unsigned short usDataLen;	· Number of bytes in the commu nication buffer.

The function returns LRC of *unsigned chart* type.

```
static unsigned charLRC (outMsg, usDataLen)
unsigned char* outMsg                     /* buffer to calculate LRC*/
unsigned short usDataLen;                 /* number of bytes in the buffer*/
{                                         /* LRC unitialization*/
    unsigned char uchLRC = 0
    while (usDataLen- -)
          uchLRC +=*outMsg++;             /* add the buffer byte without
                                          transfer*/
return ((unsigned char) (-(char uchLRC)));  /* return the sum in the comple-
                                          tion code up two */
}
```

An example of function in C language calculating the CRC sum is presented below.

All possible values of CRC sum are placed in two tables.

The first table includes the highest byte of all 256 possible values of the 16-bit CRC field, however the second table includes the lowest byte.

The assignment of the CRC sum through tabel indexing is further more rapid than the calculation of a new CRC value for each sign of the communication buffer.

Note: The below function represents bytes of the sum CRC higher/lower, and this way the CRC value returned by the function can be directly placed in the communication buffer.

The function serving to calculate CRC has two arguments:

unsigned char puchMsg*	Pointer for the communication buffer including binary data from which one must calculate LRC.
unsigned short usDataLen;	Number of bytes in the communication buffer.

The function returns CRC of *unsigned short* type.

```
        unsigned short CRC16 (puchMsg, usDataLen)
        unsigned char* puchMsg;              /* Buffer to calculate CRC*/
        unsigned short usDataLen             /* Number of bytes in the buffer*/
{
          unsigned char uchCRChi = 0xFF     /*Initialization of the higher CRC byte*/
          unsigned char uchCRClo = 0xFF     /*Initialization of the lower CRC byte*/
        while (usDataLen—)
        {       uIndex =        uchCRChi ^ *puchMsg++;    /*  CRC calculation*/
                uchCRChi = uchCRClo ^ crc_hi[uIndex];
                uchCRClo = crc_lo[uIndex];
        }
        return(uchCRChi<<8 | uchCRClo);
}

//older CRC byte table/
const unsigned char crc_hi[ ]={
 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41,  0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81,
 0x40, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0,
 0x80, 0x41, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x00, 0xC1, 0x81, 0x40, 0x01,
 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x01, 0xC0, 0x80, 0x41,
 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x00, 0xC1, 0x81,
 0x40, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x01, 0xC0,
 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x01,
 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40,
 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81,
 0x40, 0x00, 0xC1, 0x81, 0x40,0x01,  0xC0, 0x80, 0x41, 0x00, 0xC1,0x81,  0x40, 0x01, 0xC0,
 0x80, 0x41, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x00, 0xC1, 0x81, 0x40, 0x01,
 0xC0, 0x80, 0x41, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41,
 0x00, 0xC1, 0x81, 0x40, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81,
 0x40, 0x01, 0xC0, 0x80, 0x41, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0,
 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x01,
 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81, 0x40, 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41,
 0x00, 0xC1, 0x81, 0x40, 0x01, 0xC0, 0x80, 0x41, 0x01, 0xC0, 0x80, 0x41, 0x00, 0xC1, 0x81,
 0x40
};
```

//lower CRC byte table/
const unsigned char crc_lo[ ]={

```
0x00, 0xC0, 0xC1, 0x01, 0xC3, 0x03, 0x02, 0xC2, 0xC6, 0x06, 0x07, 0xC7, 0x05, 0xC5, 0xC4,
0x04, 0xCC, 0x0C, 0x0D, 0xCD, 0x0F  0xCF, 0xCE, 0x0E, 0x0A, 0xCA, 0xCB,0x0B,  0xC9, 0x09,
0x08, 0xC8, 0xD8, 0x18, 0x19, 0xD9, 0x1B, 0xDB, 0xDA, 0x1A, 0x1E, 0xDE, 0xDF, 0x1F, 0xDD,
0x1D, 0x1C, 0xDC, 0x14, 0xD4, 0xD5, 0x15, 0xD7, 0x17, 0x16, 0xD6, 0xD2, 0x12, 0x13, 0xD3,
0x11, 0xD1, 0xD0, 0x10, 0xF0, 0x30, 0x31, 0xF1, 0x33, 0xF3, 0xF2, 0x32, 0x36, 0xF6, 0xF7,
0x37, 0xF5, 0x35, 0x34, 0xF4, 0x3C, 0xFC, 0xFD, 0x3D, 0xFF, 0x3F, 0x3E, 0xFE, 0xFA, 0x3A,
0x3B, 0xFB, 0x39, 0xF9, 0xF8, 0x38, 0x28, 0xE8, 0xE9, 0x29, 0xEB, 0x2B, 0x2A, 0xEA, 0xEE,
0x2E, 0x2F, 0xEF, 0x2D, 0xED, 0xEC,0x2C, 0xE4, 0x24, 0x25, 0xE5, 0x27, 0xE7, 0xE6, 0x26,
0x22, 0xE2, 0xE3, 0x23, 0xE1, 0x21, 0x20, 0xE0, 0xA0, 0x60, 0x61, 0xA1, 0x63, 0xA3, 0xA2,
0x62, 0x66, 0xA6, 0xA7, 0x67, 0xA5, 0x65, 0x64, 0xA4, 0x6C, 0xAC, 0xAD, 0x6D, 0xAF, 0x6F,
0x6E, 0xAE, 0xAA, 0x6A, 0x6B, 0xAB, 0x69, 0xA9, 0xA8, 0x68, 0x78, 0xB8, 0xB9, 0x79, 0xBB,
0x7B, 0x7A, 0xBA, 0xBE, 0x7E, 0x7F, 0xBF, 0x7D, 0xBD, 0xBC, 0x7C, 0xB4, 0x74, 0x75, 0xB5,
0x77, 0xB7, 0xB6, 0x76, 0x72, 0xB2, 0xB3, 0x73, 0xB1, 0x71, 0x70, 0xB0, 0x50, 0x90, 0x91
0x51, 0x93, 0x53, 0x52, 0x92, 0x96, 0x56, 0x57, 0x97, 0x55, 0x95, 0x94, 0x54, 0x9C, 0x5C,
0x5D, 0x9D, 0x5F, 0x9F, 0x9E, 0x5E, 0x5A, 0x9A, 0x9B, 0x5B, 0x99, 0x59, 0x58, 0x98, 0x88,
0x48, 0x49, 0x89, 0x4B, 0x8B, 0x8A, 0x4A, 0x4E, 0x8E, 0x8F, 0x4F, 0x8D, 0x4D, 0x4C, 0x8C,
0x44, 0x84, 0x85, 0x45, 0x87, 0x47, 0x46, 0x86, 0x82, 0x42, 0x43, 0x83, 0x41, 0x81, 0x80,
0x40
```

};

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